What is claimed:

1. In a system having first and second processors, a method of synchronizing the first processor with the second processor, comprising the steps of:

(a) storing in a register parallel bits of data from the first processor, wherein at least one bit of data is a logic ONE,

(b) forming an output signal from the at least one bit of data in the register, and

(c) sending the output signal to an interrupt terminal of the second processor for synchronizing the first processor with the second processor.

2. The method of claim 1 wherein the register is a memory mapped register.

3. The method of claim 1 wherein the register is an off-core register.

4. The method of claim 1 wherein at least one of the first and second processors is a digital signal processor (DSP).

5. The method of claim 1 wherein step (b) includes detecting a leading edge of the at least one bit of data to form the output signal.

6. The method of claim 5 wherein step (c) includes sending the output signal on a dedicated line between the register and the interrupt terminal.

7. The method of claim 6 wherein the output signal is active for a duration of a clock period.

8. The method of claim 1 including the steps of

enabling the register during a write cycle, and

storing the parallel bits of data when an address of the register matches a predetermined address.

9. A system for providing an interrupt signal from a first processor to a second processor comprising

a data bus coupled to the first processor for routing parallel bits of data,

a register coupled to the data bus for storing the parallel bits of data, at least one of the parallel bits of data having an active logic level,

an edge detector coupled to the register for detecting active logic levels stored in the register and converting each active logic level into an interrupt signal, and

at least one line coupled between the edge detector and an interrupt terminal of the second processor for routing one of the interrupt signals to the interrupt terminal.

10. The system of claim 9 wherein the register includes a first set of flip/flops, each flip/flop storing one of the active logic levels, and

the edge detector includes a second set of flip/flops, each flip/flop detecting one of the active logic levels.

11. The system of claim 9 further including

an address bus coupled between the first processor and the register, and

a predetermined address for the register,

wherein the first processor routes the parallel bits of data to the register by setting the predetermined address on the address bus.

12. The system of claim 9 wherein the register is an off-core register and is enabled by a write strobe signal from the first processor.

13. The system of claim 9 wherein at least one of the first and second processors is a DSP.

14. In a multi-processor system having data lines between each processor and at least one interrupt terminal in each processor, a system for synchronizing a first processor with a second processor comprising

a register coupled to the data lines for storing data bits from the first processor, each data bit representing an interrupt signal,

a detector for detecting each of the data bits in the register, and

a signal router for routing each of the detected data bits to a respective interrupt terminal in the second processor,

wherein when the first processor stores a data bit in the register, the router provides an interrupt signal to the second processor.

15. The system of claim 14 wherein the register includes a first set of flip/flops, each flip/flop storing one of the data bits, and

the detector includes a second set of flip/flops, each flip/flop detecting one of the data bits in the register.

16. The system of claim 14 wherein the signal router includes a set of lines, each line connected to the respective interrupt terminal.

17. The system of claim 14 wherein at least one processor is a DSP.

18. The system of claim 14 further including an address bus coupled to the register, wherein the data bits are stored in the register when the first processor addresses the register.

19. The system of claim 14 wherein the data bits are stored in the register during a first clock cycle and the data bits are detected by the detector during a second clock cycle, and

the interrupt signal is enabled for a duration of a clock cycle.

20. In an integrated circuit including at least two processors, data lines between each processor, and at least one interrupt terminal in each processor, a system for synchronizing a first processor with a second processor comprising

a register coupled to the data lines for storing data bits from the first processor, each data bit representing an interrupt signal,

a detector for detecting each of the data bits in the register, and

a signal router for routing each of the detected data bits to a respective interrupt terminal in the second processor,

wherein when the first processor stores a data bit in the register, the router provides an interrupt signal to the second processor.

21. The system of claim 20 wherein the register includes a first set of flip/flops, each flip/flop storing one of the data bits, and

the detector includes a second set of flip/flops, each flip/flop detecting one of the data bits in the register.

22. The system of claim 20 wherein the signal router includes a set of lines, each line connected to the respective interrupt terminal.

23. The system of claim 20 wherein at least one processor is a DSP.

24. The system of claim 20 wherein at least one processor is a microprocessor.

25. The system of claim 20 further including an address bus coupled to the register, wherein the data bits are stored in the register when the first processor addresses the register.

26. The system of claim 20 wherein the data bits are stored in the register during a first clock cycle and the data bits are detected by the detector during a second clock cycle, and

the interrupt signal is enabled for a duration of a clock cycle.